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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,431	07/02/2001	Yuri Granik	MEGC117332	1914
26389 7590 02/15/2007 CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC 1420 FIFTH AVENUE SUITE 2800 SEATTLE, WA 98101-2347			EXAMINER	
			STEVENS, THOMAS H	
			ART UNIT	PAPER NUMBER
			2121	
SHORTENED STATUTOR	RY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)				
	09/898,431	GRANIK ET AL.				
Office Action Summary	Examiner	Art Unit				
	Thomas H. Stevens	2121				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period was reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	I. lely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 22 Ja						
,	action is non-final.					
/	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) ⊠ Claim(s) 1-14 and 16-25 is/are pending in the a 4a) Of the above claim(s) is/are withdray 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 1-14 and 16-25 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or	vn from consideration.					
Application Papers						
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acce Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex	epted or b) objected to by the liderawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
	•					
Attachment(s)	4) Interview Summary	(PTO 413)				
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 	4)	ate				

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DETAILED ACTION

- 1. Claims 1-25 were previously examined.
- 2. Claims 15-19 were canceled.
- 3. Claims 1-14,16-25 were examined.

Section I: Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 02/13/2006 has been entered.

Section II: Non-Final Rejection

Claim Objections

- 5. The examiner has provided a number of claim deficiency examples that could cause antecedent problems; however, the list may not be inclusive. Applicants should refer to these as examples of deficiencies and should make all necessary corrections.
 - Claim 1, line 3, delete "the" with the word "an"
 - Claim 2, line 1, change "the additional" to "an additional"
 - Claim 5, line 3, after "simulation of" delete the word "the"
 - Claim 5, line 4, after "from" replace "the" to "an"

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- Claim 5, line 5, after "applying" replace "the" to "a"
- Claim 8, line 4, delete the word "the"
- Claim 8, line 5, delete the word "the"
- Claim 12, line 5, after "from" replace "the" with "an"
- Claim 12, line 5, after "applying" replace "the" with "a"
- Claim 20, line 2, after "of" replace "the" with "an"
- Claim 20, line 3, after "to" delete the word "the"
- Claim 20, line 4, after "using" delete the word "the"
- Claim 20, line 4, after "of" the word "the" replaced with "an"
- Claim 20, line 7, after "using" the word "the" replaced with "an"
- Claim 20, line 9, after "on" "the" replaced with "a"
- Claim 23, line 1, after "by", delete "the".
- Claim 23, line 2, after "of", delete "the"
- Claim 23, line 4, after "from", replace "the" to "an"
- Claim 23, line 4, after "applying" delete "the"
- Claim 23, line 6. delete "the"

All claims have been treated on their merits.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

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granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1-4,8-11, 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Anderson et al., (US Patent 6,415,421; hereafter Anderson). Anderson teaches an integrated verification and manufacturability tool provides more efficient verification of integrated device designs (abstract).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim 1. A method of compensating (column 8, lines 25-30) mask/reticle data (column 8, lines 25-30 and 63-67) for lithographic (column 4, lines 8-15) process distortions (column 2, lines 2-5), comprising the acts of: reading (column 3, lines 22-28) a set of mask/reticle data (column 8, lines 25-30 and 63-67) that defines at least one feature to be created lithographically (column 4, lines 8-15); performing a simulation (column 3, line 24) of the etch (column 2, lines 2-4)effects that would occur if a wafer (column 9, line 19) is created using a mask/reticle (column 8, lines 25-30 and 63-67) corresponding to the set of mask/reticle data (column 8, lines 25-30 and 63-67); using the results of the etch (column 2, lines 2-4) simulation (column 3, line 24) to compensate features

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(column 8, lines 25-30) within the set of mask/reticle data (column 8, lines 25-30 and 63-67) for etch (column 2, lines 2-4) distortions (column 2, lines 2-5) that would occur during lithographic (column 4, lines 8-15) processing; and performing optical process correction (OPC) (column 3, line 22) to compensate (column 8, lines 25-30) for optical/resist process distortions (column 2, lines 2-5) using the etch (column 2, lines 2-4) compensated set (column 8, lines 25-30) of mask/reticle data (column 8, lines 25-30 and 63-67) as an input (column 4, lines 57-59).

Claim 2. The method of Claim 1, comprising the additional act of exporting the OPC compensated (column 8, lines 25-30) set of mask/reticle data (column 8, lines 25-30 and 63-67) to a mask/reticle writer (column 3, lines 22-28) to manufacture (title) a corresponding mask/reticle(column 8, lines 25-30 and 63-67).

Claim 3. The method of Claim 1, in which the act of performing a simulation (column 3, line 24) includes accessing a set of predetermined rules (abstract: line 7) for the etch (column 2, lines 2-4)process.

Claim 4. The method of Claim 1, in which the act of performing a simulation (column 3, line 24) includes accessing a table of predetermined values (column 10, lines 60-65) for the etch (column 2, lines 2-4) process.

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Claim 8. A computer-readable media having a sequence of programmed instructions stored thereon that when executed by a computer causes the computer to perform the acts of: reading (column 3, lines 22-28) a set of mask/reticle data (column 8, lines 25-30 and 63-67)that defines at least one feature to be created lithographically (column 4, lines 8-15); performing a simulation (column 3, line 24) of the etch (column 2, lines 2-4)effects that would occur if a wafer (column 9, line 19) is created using a mask/reticle corresponding to the set of mask/reticle data; using the results of the etch (column 2, lines 2-4)simulation (column 3, line 24) to compensate features (column 8, lines 25-30) within set of mask/reticle data (column 8, lines 25-30 and 63-67) for etch (column 2, lines 2-4) distortions (column 2, lines 2-5) that would occur during lithographic (column 4, lines 8-15) processing; and performing optical process correction (OPC) (column 3, line 22) to compensate (column 8, lines 25-30) for optical/resist process distortions (column 2, lines 2-5) using the etch (column 2, lines 2-4) compensated set (column 8, lines 25-30) of mask/reticle data (column 8, lines 25-30 and 63-67) as an input (column 4, lines 57-59).

Claim 9. The computer-readable media of Claim 8, wherein the sequence of programmed instructions causes the computer to export OPC corrected mask/reticle data (column 8, lines 25-30 and 63-67) to a mask/reticle writer (column 3, lines 22-28) to manufacture (title) a corresponding mask/reticle.

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Claim 10. The computer readable media of Claim 8, in which the act of performing a simulation (column 3, line 24) includes accessing a set of predetermined rules (abstract: line 7) for the etch (column 2, lines 2-4)process.

Claim 11. The computer readable media of Claim 8, in which the act of performing a simulation (column 3, line 24) includes accessing a table of predetermined values (column 10, lines 60-65) for the etch (column 2, lines 2-4) process.

Claim 20. A device that is formed on a wafer (column 9, line 19) created by the acts of: reading (column 3, lines 22-28) a set of mask/reticle data (column 8, lines 25-30 and 63-67)that defines at least one feature to be created lithographic (column 4, lines 8-15)ally; performing a simulation (column 3, line 24) of the etch (column 2, lines 2-4)effects that would occur if a wafer (column 9, line 19) is created using a mask/reticle corresponding to the set of mask/reticle data; using the results of the etch (column 2, lines 2-4)simulation (column 3, line 24) to compensate features (column 8, lines 25-30) within the set of mask/reticle data (column 8, lines 25-30 and 63-67)for etch (column 2, lines 2-4)distortions (column 2, lines 2-5) that would occur during lithographic (column 4, lines 8-15) processing; performing optical process correction (OPC) (column 3, line 22) to compensate (column 8, lines 25-30) for optical/resist process distortions (column 2, lines 2-5) using the etch (column 2, lines 2-4) compensated (column 8, lines 25-30) set of mask/reticle data (column 8, lines 25-30 and 63-67) as an input (column 4, lines 57-59); exporting the OPC corrected set of mask/reticle data (column 8, lines 25-30 and

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ø,

63-67)to a mask/reticle writer (column 3, lines 22-28) to manufacture (title) a corresponding mask/reticle; and using the mask/reticle to create the device on the wafer (column 9, line 19).

Claim 21. The device of Claim 20, in which the act of performing a simulation (column 3, line 24) includes accessing a set of predetermined rules (abstract: line 7) for the etch (column 2, lines 2-4) process.

Claim 22. The device of Claim 2,0, in which the act of performing a simulation (column 3, line 24) includes accessing a table of predetermined values (column 10, lines 60-65) for the etch (column 2, lines 2-4) process.

Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
 - 1. Determining the scope and contents of the prior art.
 - 2. Ascertaining the differences between the prior art and the claims at issue.
 - 3. Resolving the level of ordinary skill in the pertinent art.

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4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

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10. Claims 5-7,12-14 and 23-25 are rejected under 35 U.S.C. 103(a) as being obvious over Anderson in view of Tejnil (US Patent Application 2002/0086218; hereafter Tejnil).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filling date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filling date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Per claims 5,6, 12, and 23 Anderson teaches

- method of compensating (column 8, lines 25-30)
- mask/reticle data (column 8, lines 25-30 and 63-67)
- for lithographic (column 4, lines 8-15) process distortions (column 2, lines 2-5),

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 reading (column 3, lines 22-28) a set of mask/reticle data(column 8, lines 25-30 and 63-67)

- defines at least one feature to be created lithographically (column 4, lines 8-15);
 performing a simulation (column 3, line 24) of the etch (column 2, lines 2-4)effects that would occur if a wafer (column 9, line 19)
- corresponding to the set of mask/reticle data (column 8, lines 25-30 and 63-67);
 calculating etch (column 2, lines 2-4)
- loop that adjusts the mask/reticle data (column 8, lines 22-30) for optical/resist process distortions (column 2, lines 2-5)
- programmed instructions (column 12, lines 47-50)
- executed by a computer causes the computer to perform (column 3, lines 57-58 with figure 6)

but fails to teach biases to which Tejnil teaches

Per claims 5, 12, and 23 Tejnil teaches

- biases ("any process biasing" paragraph 0028)
- biases from the etch ("any process biasing" paragraph 0028)

Therefore it would have been obvious to a person having ordinary skill in the art at the time of applicants' invention to modify Anderson by way of Tejnil because Tejnil teaches a method of improving definition of a project feature with a two-mask exposure

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process in lithography (paragraph 0017) and to enhance the definition of the product features separated by the narrow space (paragraph 0018).

Per claims 6, 13 and 24 Anderson teaches

a set of predetermined rules (abstract: line 7) for the etch (column 2, lines 2-4)
 process.

Per claims 7, 14, and 25 Anderson teaches

 accessing a table of predetermined values (column 5, lines 8-18 ""hierarchical representation of edges") for the etch (column 2, lines 2-4) process

Section III: Response to Arguments

11. Applicant's arguments, see pages 7-9 filed 12/05/2005, with respect to the rejection(s) of claim(s)1-25 (previous) under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejections is made in view of Anderson (102e) and in view of Tejnil (103a).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

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JP 62057216 teaches a method to obtain an electron beam lithography apparatus, which can correct the distortion in the

optical system of an exposure device, even if the object of the lithography is a mask or a reticle by storing the correcting

values of the masks and reticle in a computer

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-

3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact

examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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Center (EBC) (toll-free (866-217-9197)).

Anthony Knight Supervisory Patent Examiner Tech Center 2100